UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/406,788	09/28/1999	BAT-SHEVA OVADIA	023826/0141	1937

27130 7590 02/11/2004

EITAN, PEARL, LATZER & COHEN ZEDEK LLP
10 ROCKEFELLER PLAZA, SUITE 1001
NEW YORK, NY 10020

EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	18

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/406,788	OVADIA ET AL.	
	Examiner	Art Unit	
	Kevin M Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-8,10,12,19-23,27,28,30,32 and 39-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,10,12,19-23,27,28,30,32 and 39-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. This office action, in response to the amendment filed 11/17/2003, is a final office action.

Response to Arguments

2. Applicant's arguments, see the remarks, filed 11/17/2003, with respect to the rejections of claims 1-3, 6 and 7 under 35 USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration of the newly added limitations, new grounds of rejection is made in view Alidina et al (US 5,987,490) in view of Asano et al (US 5,715,470).

Applicant's arguments filed 11/17/2003 have been fully considered but they are not persuasive.

Applicant states, in regards to claim 8, 10, 12 and 19-23, the prior art does not discloses a storage device having memory cells to store all of the race back bits. However, Alidina discloses a storage device comprising two registers 46 shown in figure 3 that store all of the traceback bits. These rejections are maintained and stated below.

Applicant states, regarding claims 27, 28, 30, 32 and 39-43, the prior art does not disclose storing the trace bits in sequential order in a group of memory cells. However, the storage device's registers are shift in data when data is available and the register is enabled. This data will be stored in the order it is input to the register (column 5, lines 19-33). The rejections to these claims are maintained and stated below.

Applicant has added new claims 44-54. Rejections of these claims are stated below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 45-54 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has used the term "B-bit" and "B" and this term is not found in the specifications as originally filed.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 states, "said at least one arithmetic logic unit" in claim 7. This limitation contradicts claim 1 where no more than one unit is claimed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 8, 10, 12, 19-23, 27, 28, 30, 32 and 39-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Alidina et al (US 5,987,490).

Regarding claims 8, 10 and 12, Alidina discloses a system and method for decoding Viterbi codes as shown in figure 3. Alidina discloses a storage device comprising two registers 46 that store all of the traceback bits. The storage device's registers are shift in data when data is available and the register is enabled. This data will be stored in the order it is input to the register (column 5, lines 19-33).

Regarding claims 19 and 39, Alidina discloses a system and method for decoding Viterbi codes as shown in figure 3. Alidina discloses storing traceback bits in a pair of registers 46.

Regarding claims 20-23, 28, 30, 32 and 40-43, Alidina discloses a portion of the bits is stored in register ar0 and a portion of the bits is stored in ar1. The register will comprise a number of memory storage components.

Regarding claim 27, Alidina discloses a storage device comprising two registers 46 that store all of the traceback bits. The storage device's registers are shift in data

when data is available and the register is enabled. This data will be stored in the order it is input to the register (column 5, lines 19-33).

Regarding claim 44, Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits.

Regarding claim 45, Alidina discloses the trace back bit is stored as the least significant bit then the data is left shifted when new data is available and this new trace back bit is stored.

Regarding claim 46, the add compare select circuit is shown in figure 3 and the trace bits are input to the registers.

Regarding claims 47-49, the trace back bits are stored in the registers along with previous bits.

Regarding claim 50, the contents of the registers are accessed and the data is recovered.

Regarding claims 51, 52 and 54, Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits. Alidina discloses the trace back bit is stored as the least significant bit then the data is left shifted when new data is available and this new trace back bit is stored.

Regarding claim 53, the add compare select circuit is shown in figure 3 and the trace bits are input to the registers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al (US 5,987,490) in view of Asano et al (US 5,715,470).

Regarding claim 1, Alidina discloses a system and method for decoding Viterbi codes as shown in figure 3. Alidina discloses a storage device comprising two registers 46 that store all of the traceback bits. The storage device's registers are shift in data when data is available and the register is enabled. Alidina does not disclose using only one arithmetic logic unit. Asano discloses using only one ALU and inputting the trace bits to a pair of registers (figure 6 and column 5, lines 41-47). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the use of one ALU as taught by Asano into the system of Alidina to minimize the size and the number of circuitry components in the system.

Regarding claim 2, Alidina discloses this data will be stored in the order it is input to the register (column 5, lines 19-33).

Regarding claim 3, the registers store half of the trace back bits

Regarding claim 6, the registers are shift registers (Alidina: column 5, lines 19-32)

Regarding claim 7, Asano discloses a barrel shifter receiving the output of the ALU and sending a signal to the registers.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications; please mark "EXPEDITED PROCEDURE" or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
2/5/2004

KHAI TRAN
PATENT EXAMINER
2/6/04